WHAT IS CLAIMED IS:

1. A semiconductor device comprising an N channel metal oxide semiconductor (MOS) transistor, the N channel MOS transistor including:

a P type semiconductor substrate;

an N type epitaxial region formed on the P type semiconductor substrate;

a first P type buried layer isolating the N type epitaxial region from another N type epitaxial region;

an N well formed in the N type epitaxial region;

a drain region formed in the N well;

a P well surrounding side faces of the N well so as to be separated from the N well;

a source region formed in the P well;

a gate formed on each upper layer portion of the drain region and the source region;

a second P type buried layer formed below the N well and the P well so as to be joined to the P well and to be separated from the P type semiconductor substrate and the first P type buried layer; and

an N type buried layer formed so as to be joined to the second P type buried layer and the P type semiconductor substrate and to be separated from the P well, the N well, and the first P type buried layer,

wherein a first electrode electrically connected to the N type epitaxial region, a second electrode electrically connected to the P type semiconductor substrate, and a third electrode electrically connected to

the first P type buried layer are connected to ground potential.

2. The semiconductor device according to claim 1, wherein a connection is established between the first electrode and the ground potential so as to be able to apply a power supply potential to the N type epitaxial region.

3. The semiconductor device according to claim 1, wherein the source region is formed in a first N type semiconductor region, and a fourth electrode electrically connected to the source region is joined to the first N type semiconductor region and a first P type semiconductor region surrounding the first N type semiconductor region and is separated from the P well.

4. The semiconductor device according to claim 1, wherein the drain region is formed in a second N type semiconductor region.

5. The semiconductor device according to claim 1, wherein the first electrode is joined to a third N type semiconductor region formed in the N type epitaxial region and is separated from the N type epitaxial region.

6. The semiconductor device according to claim 1, wherein the second electrode is joined to a second P type semiconductor region formed in the first P type buried layer and is separated from the first P

type buried layer.

7. The semiconductor device according to claim 1, wherein a switching element forming an inverter as a motor driver includes the N channel MOS transistor.